

PHASE CONTROL THYRISTOR

AT975

Repetitive voltage up to

5200 V

Mean on-state current

3965 A

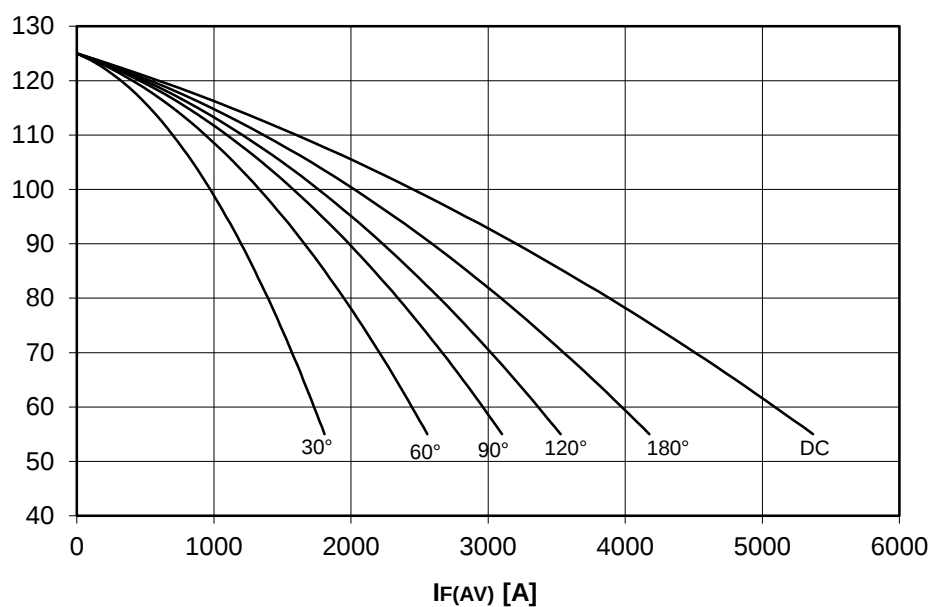
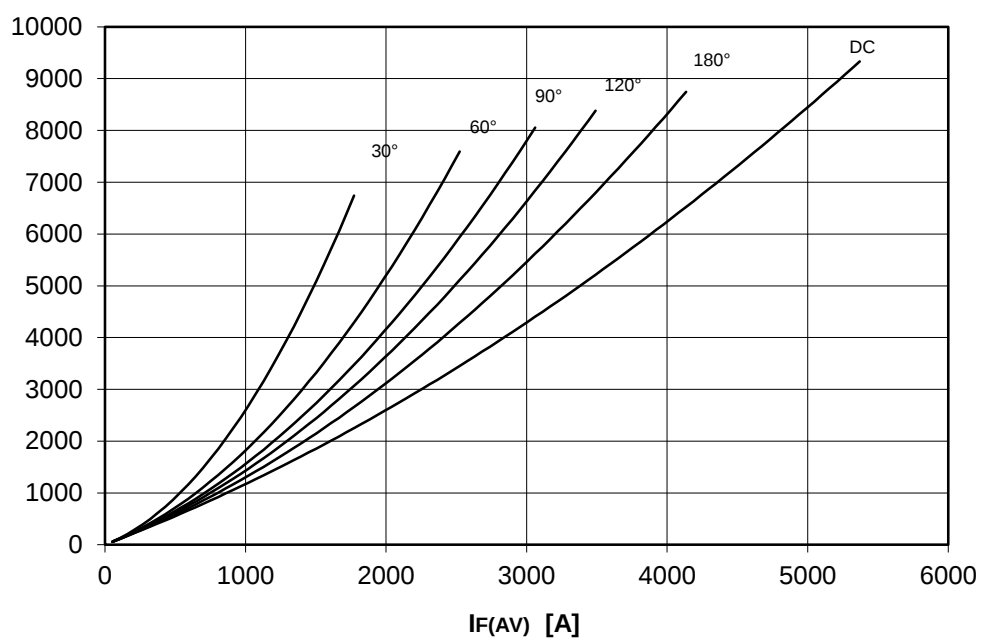
Surge current

60 kA

FINAL SPECIFICATION

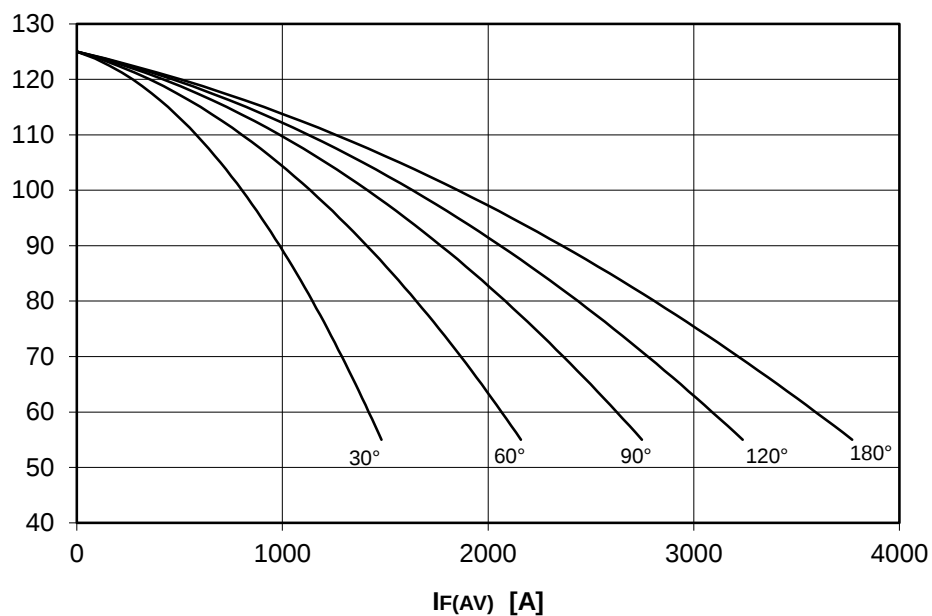
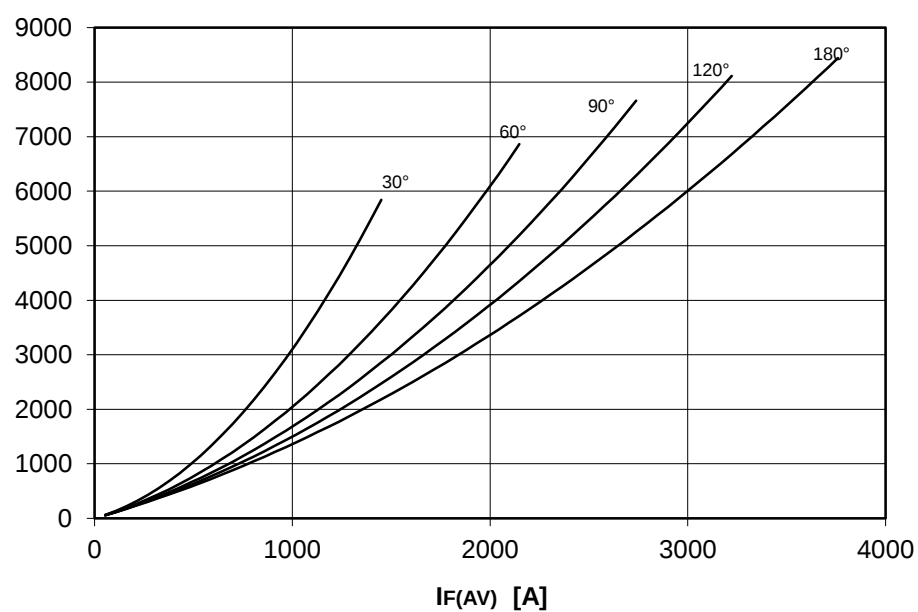
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Symbol	Characteristic	Conditions	T _j [°C]	Value	Unit
BLOCKING					
V _{RRM}	Repetitive peak reverse voltage		125	5200	V
V _{RSM}	Non-repetitive peak reverse voltage		125	5300	V
V _{DRM}	Repetitive peak off-state voltage		125	5200	V
I _{RRM}	Repetitive peak reverse current	V=VRRM	125	300	mA
I _{DRM}	Repetitive peak off-state current	V=VDRM	125	300	mA
CONDUCTING					
I _{T (AV)}	Mean on-state current	180° sin, 50 Hz, T _c =70°C, double side cooled		3965	A
I _{TSM}	Surge on-state current	sine wave, 10 ms	125	60.0	kA
I ² t	I ² t	without reverse voltage		18000 x1E3	A²s
V _T	On-state voltage	On-state current = 3000 A	25	1.50	V
V _{T(TO)}	Threshold voltage		125	1.04	V
r _T	On-state slope resistance		125	0.130	mohm
SWITCHING					
di/dt	Critical rate of rise of on-state current, min.	From 67% VDRM, gate 10V 5ohm	125	200	A/μs
dv/dt	Critical rate of rise of off-state voltage, min.	Linear ramp up to 67% of VDRM	125	1000	V/μs
t _d	Gate controlled delay time, typical	VD=0.4 VRM, IGM=2 A	25	3	μs
t _q	Circuit commutated turn-off time, typical	dv/dt = 20 V/μs linear up to 75% VDRM	125	400	μs
Q _{RR}	Reverse recovery charge	IT=2100 A, di/dt = 3 A/μs, VR=100 V		4500	μC
I _{RR}	Peak reverse recovery current			150	A
t _{RR}	Reverse Recovery Time			60	μs
I _H	Holding current, typical	VD=5V, gate open circuit	25	500	mA
I _L	Latching current, typical	VD=12V, tp=50μs	25	1500	mA
GATE					
V _{GT}	Gate trigger voltage	VD=12V	25	2.5	V
I _{GT}	Gate trigger current	VD=12V	25	250	mA
V _{GD}	Non-trigger gate voltage, min.	VD=67%VDRM	125	0.25	V
V _{FGM}	Peak gate voltage (forward)			10	V
I _{FGM}	Peak gate current			10	A
V _{RGM}	Peak gate voltage (reverse)			10	V
P _{GM}	Peak gate power dissipation	Pulse width 100 μs		150	W
P _G	Average gate power dissipation			3	W
MOUNTING					
R _{th(j-c)}	Thermal impedance, DC	Junction to case, double side cooled		6.0	°C/kW
R _{th(c-h)}	Thermal impedance	Case to heatsink, double side cooled		1.5	°C/kW
T _j	Operating junction temperature			-30 / 125	°C
F	Mounting force			80.0 / 100.0	kN
	Mass			3000	g
ORDERING INFORMATION : AT975 S 52					
standard specification ☐ VDRM&VRRM/100 ☐					

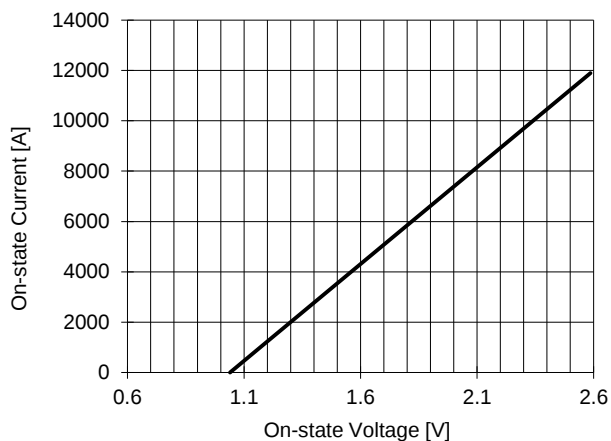
DISSIPATION CHARACTERISTICS**SQUARE WAVE****Th [°C]****PF(AV) [W]**

DISSIPATION CHARACTERISTICS

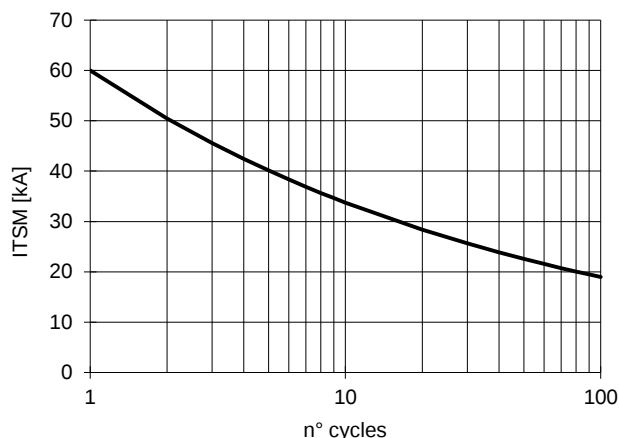
SINE WAVE

Th [°C]**PF(AV) [W]**

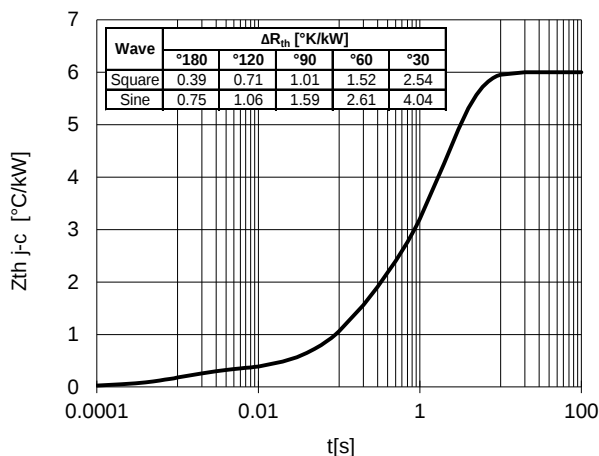
ON-STATE CHARACTERISTIC
 $T_j = 125^\circ\text{C}$



SURGE CHARACTERISTIC
 $T_j = 125^\circ\text{C}$

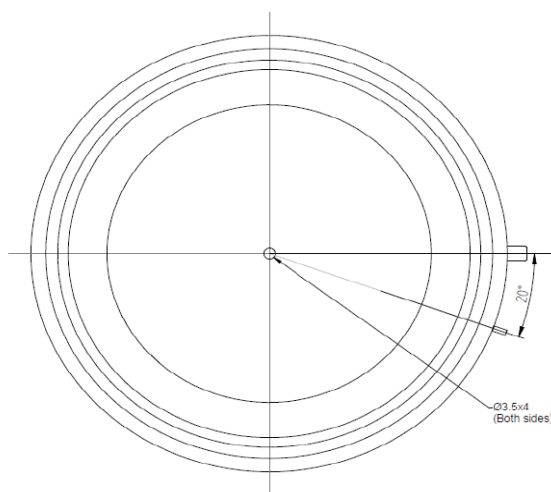
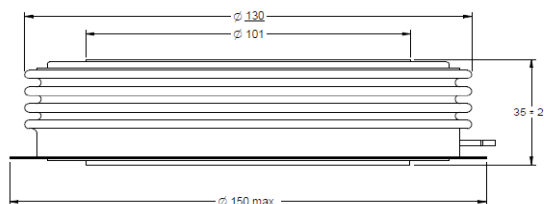


TRANSIENT THERMAL IMPEDANCE
DOUBLE SIDE COOLED



$$Z_{th j-c}(t) = \sum_{i=1}^n A_i * \left(1 - e^{-\frac{t}{\tau_i}}\right)$$

i	1	2	3	4
$A_i [^\circ\text{C/kW}]$	2.738	1.779	1.186	0.297
$\tau_i [s]$	2.4	1.70	0.16	0.001



Dimensions
in mm



Cathode terminal type DIN 46244 - A 4.8 - 0.8

Gate terminal type AMP 60598 - 1

All the characteristics given in this data sheet are guaranteed only with uniform clamping force, cleaned and lubricated heatsink, surfaces with flatness $< .03 \text{ mm}$ and roughness $< 2 \mu\text{m}$.

In the interest of product improvement POSEICO SpA reserves the right to change any data given in this data sheet at any time without previous notice.

If not stated otherwise the maximum value of ratings (symbols over shaded background) and characteristics is reported.

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